

# Liang-Kai (Mike) Wang

---

2801 Manlove Rd #11, Sacramento, CA 95826, (608) 628-5849, [lwang@cae.wisc.edu](mailto:lwang@cae.wisc.edu)

## Research Interest

Major in computer engineering and architecture. Special interests in algorithm development and implementation for computer arithmetic, RTL design and verification, and tool development for SoC testing.

## Education

**PhD Student**, Sep 2003 - present

**University of Wisconsin** - Madison WI

**M.S. Computer Engineering**, December 2003, **GPA: 3.8**

*Relevant Courses Completed:* Advanced Computer architecture, VLSI System Design, Digital System Design and Synthesis, Testing and Testable Design of Digital Systems, Digital Circuits and Components, Digital Engineering Lab, Embedded System, and Design Automation of Digital System

**National Chiao Tung University**, Hsinchu, Taiwan

**B.S. Electronic Engineering**, June 1999, **GPA 3.8**

## Experience

**Intel Corporation, Folsom CA**. Design for testing team in Cellular and Handheld devices Group  
**Co-op**, May 2004-present

Developing functional self-testing generation tool for cellular processors.

**University of Wisconsin-Madison**, Dept. of Electrical & Computer Engineering

**Teaching Assistant**, January 2004 ~ May 2004

Led discussion for ECE 555, Digital Circuits and Components

**Research Assistant**, September 2003 ~ Present (Advisor: Professor Michael Schulte)

Developing and implementing algorithms for decimal division and square root.

**Research Assistant**, September 2002 ~ Jan 2003 (Advisor: Professor Charlie Chen)

Designed Han-Carlson Adder through substrate-biasing with TSMC 0.18um technology.

## Research Projects

**Hardware Support for 1GHz 16-digit Decimal Fixed-Point Arithmetic** (Fall 2002)

Designed fixed-point decimal addition/subtraction logic by Cadence Design Kit (CDK) with TSMC 0.18um Bulk CMOS technology.

**High Speed Han-Carlson Adder with substrate-biasing** (Summer, Fall 2002)

Implemented Han-Carlson Adder with clock frequency up to 3GHz in schematic captures

**Hardware Support for 16-bits Decimal Fixed-Point Arithmetic** (Fall 2002)

Design the fixed-point decimal addition/subtraction logic by 10's complement.

## Publication

L.- K. Wang and Michael J. Schulte, "Decimal Floating-Point Division Using Newton-Raphson Iteration", in *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, Galveston, Texas, September, 2004

## Academic Projects

**Introduction to Information Security** (Spring 2004)

Designed on-line poker system by using XML and OpenSSL/OpenGL library.

**Advanced Computer Architecture** (Spring 2004)

Implemented Cyclone: a broadcast-free dynamic instruction scheduler with selective replay. By using SimpleScalar simulator.

**Digital Engineering Lab** (Spring 2003)

Implemented FPGA-based VoIP machine using Xilinx XSV-800.

**Embedded System** (Spring 2003)

Designed FPGA-based 128/196/256 bits Twofish cipher with key scheduler and controller.

**Digital System Design and Synthesis** (Fall 2002)

Implemented RC6 Encryption/Decryption Algorithm in Verilog.

**VLSI System Design** (in Computer Science Department, Spring 2002)

VLSI design of a 4-port Crossbar Switch based on Virtual-Output-Queuing

**Digital Circuits and Components** (Spring 2002) *Best team of the class for the final project*

Standard Cell Design of Add/Shift Sequential Multiplier using Mentor Graphic tools.

**Computer Architecture Design** (Fall 2001)

Designed MIP2000 16-bit multi-cycle microprocessor.

**Testing and Testable Design of Digital System** (Fall 2001)

Developed complete, economical test sets to diagnose faulty circuits using ATPG testing tool.

**Skills**

**Languages:** Proficient programming in Verilog, Perl, and C/C++.

**CAD Tools:** Extensive experience with Cadence, Mentor Graphics, and Synopsys tool sets.